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| **First Named Inventor** | Shunpei YAMAZAKI et al. |
| **Group Art Unit** | 2813 |
| **Examiner Name** | T. Nguyen |
| **Attorney Docket Number** | 0756-7199 |

## ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
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- ☐ Petition
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- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ After Allowance Communication to Group
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- ☐ Status Letter
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  1. Verification of Translation/English Translation comprising 48 pages of JP-2002-276295 filed 09/20/2002
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**Remarks**

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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| Date | 10-4-05 |

## CERTIFICATE OF MAILING

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Attorney Docket No. 0756-7199

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | |
|---|---|---|
| In re Patent Application of: | ) | Group Art Unit: 2813 |
| Shunpei YAMAZAKI et al. | ) | Examiner: T. Nguyen |
| Serial No. 10/664,962 | ) | CERTIFICATE OF MAILING |
| Filed: September 22, 2003 | ) | I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 10-4-05. |
| For: DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF | ) | Adam Stamper |

**SUBMISSION OF VERIFICATION OF TRANSLATION**

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Further to the Amendment filed on August 29, 2005, Applicant submits herewith a verified English translation of priority Japanese Application No. 2002-276295 filed September 20, 2002.

Applicant respectfully submits that the 102 and 103 rejections have been overcome with the submission of the verified English translation. Reconsideration and withdrawal of the rejections under 102 and 103 is requested.

Respectfully submitted,

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Attorney Docket No.:0756-7199

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re Patent Application of | ) |
| Shunpei Yamazaki et al. | ) Examiner: T.NGUYEN |
| Application No.: 10/664,962 | ) Art Unit: 2813 |
| Filed: September 22, 2003 | ) |
| For: DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF | ) |

Commissioner for Patents

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VERIFICATION OF TRANSLATION

Sir:

I, Yumiko Takekoshi, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 2002-276295 filed on September 20, 2002 and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 2002-276295 filed on September 20, 2002.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 28th day of September 2005

Yumiko Takekoshi

Name:Yumiko Takekoshi

[Name of Document] Patent Application

[Reference Number] P006619

[Filing Date] September 20, 2002

[Attention] Commissioner, Patent Office

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[List of Attachment]

[Attachment] Specification 1

[Attachment] Drawing 1

[Attachment] Abstract 1

[Proof] Required

[Name of Document] Specification

[Title of the Invention]

DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

[Scope of Claim]

[Claim 1]

A display device characterized by comprising a wiring in which a conductive film, a conductive barrier film; and a wiring containing Cu as its component are stacked,

wherein a width of the conductive film is aligned with that of the conductive barrier film, and

wherein a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film.

[Claim 2]

A display device characterized by comprising a wiring in which a conductive film, a conductive barrier film; and a wiring containing Cu as its component are stacked,

wherein a width of the conductive film is aligned with that of the conductive barrier film, and

wherein a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film, and

the wiring containing Cu as its main component is formed by sputtering using a mask.

[Claim 3]

A display device characterized by comprising a signal line and a scan line

provided to intersect with the signal line:

wherein the signal line comprises a conductive film, a conductive barrier film, and a wiring containing Cu as its main component over the conductive barrier film, and

wherein a width of the conductive film is aligned with that of the conductive barrier film, and

a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film.

[Claim 4]

A display device characterized by comprising a signal line and a scan line provided to intersect with the signal line,

wherein the scan line comprises a conductive barrier film and a wiring containing Cu as its main component over the conductive barrier film, and

wherein a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film.

[Claim 5]

A display device characterized by comprising:

a signal line and a scan line provided to intersect with the signal line:

wherein the signal line comprises a first conductive barrier film which is formed over the conductive film, and a first wiring containing Cu as its main component over the first conductive barrier film,

wherein the scan line comprises a second conductive barrier film and a second wiring containing Cu as its main component over the second conductive barrier film,

wherein a width of the conductive film is aligned with that of the first conductive barrier film, and a width of the first wiring containing Cu as its main component is narrower than that of the first conductive barrier film, and

wherein a width of the second wiring containing Cu as its main component is narrower than that of the second conductive barrier film.

[Claim 6]

A display device characterized by comprising:

a signal line;

a scan line provided to intersect with the signal line; and

a light emitting element which is formed at an intersection of the signal line and the scan line,

wherein driving current is supplied to the light emitting element through the signal line,

wherein the signal line comprises a conductive barrier film which is formed over the conductive film, and

a first wiring containing Cu as its main component over the conductive barrier film,

wherein a width of the conductive film is aligned with that of the conductive barrier film, and

a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film.

[Claim 7]

A display device characterized by comprising:

a signal line;

a scan line provided to intersect with the signal line, and

a light emitting element which is formed at an intersection of the signal line and the scan line,

wherein voltage is inputted from the signal line,

wherein the scan line comprises a conductive barrier film and a wiring containing Cu as its main component over the conductive barrier film, and

wherein a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film.

[Claim 8]

A display device characterized by comprising:

a signal line and a scan line provided to intersect with the signal line, and

a light emitting element which is formed at an intersection of the signal line and the scan line:

wherein the signal line comprises

a first conductive barrier film which is formed over the conductive film, and a first wiring containing Cu as its main component over the first conductive barrier film,

wherein the scan line comprises a second conductive barrier film and a second wiring containing Cu as its main component over the second conductive barrier film,

wherein a width of the conductive film is aligned with that of the first conductive barrier film, and a width of the first wiring containing Cu as its main component is narrower than that of the first conductive barrier film, and

wherein a width of the second wiring containing Cu as its main component is narrower than that of the second conductive barrier film.

[Claim 9]

A display device characterized by comprising:

a signal line;

a scan line provided to intersect with the signal line;

a TFT which is formed at an intersection of the signal line and the scan line; and

a light emitting element electrically connected to the TFT,

wherein voltage is inputted from the signal line,

wherein the signal line comprises

a first conductive barrier film which is formed over the conductive film, and a first wiring containing Cu as its main component over the first conductive barrier film,

wherein the scan line and a gate electrode of the TFT comprise a second conductive barrier film and a second wiring containing Cu as its main component over the second conductive barrier film,

wherein a width of the conductive film is aligned with that of the first conductive barrier film, and a width of the first wiring containing Cu as its main component is narrower than that of the first conductive barrier film, and

wherein a width of the second wiring containing Cu as its main component is narrower than that of the second conductive barrier film.

[Claim 10]

A display device characterized by comprising:

a signal line;

a scan line provided to intersect with the signal line;

a TFT which is formed at an intersection of the signal line and the scan line; and

a light emitting element electrically connected to the TFT

wherein voltage is inputted from the signal line,

the signal line and a source electrode and a drain electrode of the TFT comprise

a first conductive barrier film which is formed over the conductive film, and a first wiring containing Cu as its main component over the first conductive barrier film,

wherein the scan line and a gate electrode of the TFT comprise a second conductive barrier film and a second wiring containing Cu as its main component over the second conductive barrier film,

wherein a width of the conductive film is aligned with that of the first conductive barrier film, and a width of the first wiring containing Cu as its main component is narrower than that of the first conductive barrier film, and

wherein a width of the second wiring containing Cu as its main component is narrower than that of the second conductive barrier film.

[Claim 11]

A display device characterized by comprising a semiconductor film over an insulating surface and a gate electrode provided over the semiconductor film, and

wherein the gate electrode comprises a conductive barrier film and a wiring containing Cu as its main component over the conductive barrier film,

wherein a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film.

[Claim 12]

A display device characterized by comprising a semiconductor film provided over an insulating surface and an impurity region provided in the semiconductor film, and an electrode connected to the impurity region,

wherein the electrode comprises a conductive barrier film, and a wiring containing Cu as its main component over the conductive barrier film,

wherein a width of the conductive film is aligned with that of the conductive

film, and

wherein a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film.

[Claim 13]

A display device characterized by comprising a semiconductor film over an insulating surface;

a gate electrode over the semiconductor film,

an impurity region provided in the semiconductor film; and

an electrode connected to the impurity region and a wiring,

wherein the electrode and the wiring comprises a conductive film,

a first conductive barrier film which is formed over the conductive film,

a first wiring containing Cu as its main component over the first conductive barrier film, and

wherein the gate electrode comprises a second conductive barrier film, and a second wiring containing Cu as its main component over the second conductive barrier film,

wherein a width of the conductive film is aligned with that of the first conductive barrier film,

a width of the first wiring containing Cu as its main component is narrower than that of the first conductive barrier film, and

wherein a width of the second wiring containing Cu as its main component is narrower than that of the second conductive barrier film.

[Claim 14]

A display device characterized by comprising:

a conductive barrier film which is formed over a conductive film;

a wiring containing Cu as its main component over the conductive barrier film; and

an input terminal connected to the wiring,

wherein a width of the conductive film is aligned with that of the conductive barrier film,

wherein a width of the film containing Cu as its main component is narrower than that of the conductive barrier film, and

wherein the input terminal is not formed over the film containing Cu as its main component.

[Claim 15]

A display device characterized by comprising:

a conductive barrier film which is formed over a conductive film; and

a wiring containing Cu as its main component over the conductive barrier film; and

an input terminal connected to the wiring,

wherein a width of the conductive film is aligned with that of the conductive barrier film,

wherein a width of the film containing Cu as its main component is narrower than that of the conductive barrier film, and

wherein the wiring and the input terminal are connected through a resin containing a conductor, and

wherein the input terminal is not formed over the film containing Cu as its main component.

[Claim 16]

A display device characterized by comprising:

a conductive barrier film which is formed over a conductive film;

a wiring containing Cu as its main component over the conductive barrier film; and

an input terminal connected to the wiring,

wherein a width of the conductive film is aligned with that of the conductive barrier film,

wherein a width of the film containing Cu as its main component is narrower than that of the conductive barrier film,

wherein the wiring and the input terminal are connected through a resin containing a conductor, and

wherein an edge of the input terminal is not aligned with that of the film containing Cu as its main component.

[Claim 17]

A display device characterized by comprising:

a conductive barrier film which is formed over a conductive film; and

a wiring containing Cu as its main component over the conductive barrier film; and

an input terminal connected to the wiring,

wherein a width of the conductive film is aligned with that of the conductive barrier film,

wherein a width of the film containing Cu as its main component is narrower than that of the conductive barrier film, and

wherein the wiring is connected to a protective circuit including a semiconductor film in a connecting region of the input terminal.

[Claim 18]

A display device characterized by comprising:

a wiring including a first conductive barrier film which is formed over a conductive film;

a first wiring containing Cu as its main component over the first conductive barrier film; and

a gate wiring including a second wiring containing Cu as its main component over a second conductive barrier film; and

an input terminal connected to the wiring,

wherein a width of the conductive film is aligned with that of the first conductive barrier film,

wherein a width of the wiring containing Cu as its main component is narrower than that of the conductive barrier film, and

wherein a width of the second wiring containing Cu as its main component is narrower than that of the second conductive barrier film, and

wherein the wiring and the gate wiring are connected to a protective circuit including a semiconductor film in a connecting region of the input terminal.

[Claim 19]

A display device according to any one of claims 1 to 18 characterized in that, the conductive barrier film comprises one of TiN, TaN, TiC, TaC, and WN.

[Claim 20]

A method of manufacturing a display device according to any one of claims 1

to 3, 5, 6, 8 to 10, 12 to 19 characterized in that the conductive film comprises Ti.

[Claim 21]

A display device according to any one of claims 1 to 20 characterized in that the wiring containing Cu as its main component is covered with an insulating barrier film which is formed of one or plurality of materials selected from SiN, SiNO, AlN or $Al_xN_x$ containing nitrogen.

[Claim 22]

A method of manufacturing display device characterized by comprising the steps of:

forming a conductive barrier film over a substrate in a first deposition chamber;

transferring the substrate into a second deposition chamber without exposure to the air;

forming a wiring containing Cu as its main component over the conductive barrier film in the second deposition chamber;

transferring the substrate into a third deposition chamber without exposure to the air; and

forming an insulating barrier film over the wiring containing Cu as its main component.

[Claim 23]

A method of manufacturing display device in which a conductive film, conductive barrier film and a wiring containg Cu as its main component are stacked in order over a substrate and the an insulating barrier film is provided to cover the wiring containing Cu as its main component, characterized by comprising the steps of

forming a conductive barrier film over the substrate in a first deposition

chamber;

transferring the substrate into a second deposition chamber without exposure to the air;

forming a wiring containing Cu as its main component over the conductive barrier film,

transferring the substrate into a third deposition chamber without exposure to the air; and

forming the insulating barrier film over the wiring containing Cu as its main component,

providing a substrate and a mask by a holding means comprising a magnet in the second deposition chamber, and

forming the wiring containing Cu as its main component over the substrate with the mask therebetween.

[Claim 24]

A method of manufacturing a display device according to claim 23 characterized in that the mask has an auxiliary wiring provided not to face the substrate.

[Claim 25]

A method of manufacturing a display device characterized by comprising the steps of:

forming a semiconductor film over a substrate;

forming a gate electrode over the semiconductor film;

forming an impurity region in the semiconductor film with the gate electrode as a mask;

forming an insulating film to cover the gate electrode;

forming a contact in the insulating film; and

forming an electrode which is connected through the contact to the impurity region, and a signal line,

wherein the electrode and the signal line forms subsequently a conductive film, conductive barrier film, a wiring containing Cu as its main component with lamination,

wherein the conductive barrier film is formed in a first deposition chamber;

wherein the substrate is transferred into a second deposition chamber without exposure to the air;

wherein the wiring containing Cu as its main component is formed over the conductive barrier film;

wherein the substrate is transferred into a third deposition chamber without exposure to the air; and

wherein the insulating barrier film is formed over the wiring containing Cu as its main component.

[Claim 26]

A method of manufacturing a display device according to any one of claims 22 to 25 characterized in that the second deposition chamber comprises a target, means for cooling the target, means for moving the target up and down, and a magnet that moves parallel to the target.

[Claim 27]

A method of manufacturing a display device according to any one of claims 22 to 26 characterized in that reduced pressure is kept in the first to the third deposition chamber.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention relates to a semiconductor device that has a semiconductor element (specifically, a thin film transistor). That is, the present invention relates to an EL display device (a light emitting device) provided with a light emitting element and a liquid crystal display device and a manufacturing method there of, especially, to a large-sized display device and a manufacturing method thereof.

[0002]

[Prior Art]

These days, it has been proceeded to make a screen have a large size and a high definition in active matrix type semiconductor devices such as an EL display device and a liquid crystal display device, and the number of wirings such as signal lines and scan lines tends to increase as well as a length of the wiring. Therefore, it is required to prevent voltage drop due to wiring resistance, trouble in writing of a signal into a pixel, and trouble in gray scales.

[0003]

In the EL display device, a driving method for displaying an image with multiple gray scales has a voltage input system of inputting voltage from a signal line and a current input system of inputting current from a signal line, and further, the voltage input system has a current writing system of writing data in current format (driving current) into a light emitting element for controlling luminance and a voltage writing system of writing data in voltage format into a light emitting element for controlling luminance while the current input system has the current writing system. Such driving method especially has trouble caused due to wiring resistance. The

wiring resistance causes delay in transmission of a signal to a terminal of a signal line, and the voltage drop of a power source line (specifically, a current supply line) makes it difficult to supply predetermined current or voltage. Then, fluctuation in displaying is caused as the result since luminance of light emitted from the light emitting element is proportional to a value of the current or voltage supplied through the signal line.

[0004]

Further, due to the voltage drop, the EL display device and the liquid crystal display device have trouble of waveform distortion of a pulse signal input through the wiring.

[0005]

In the case of using copper as a material with low resistance for forming a wiring, there is a means of forming a plugged wiring (a structure formed with damascene). In the damascene, however, an insulating film is provided at the position of a wiring to be formed, a groove for forming the wiring is formed in the insulating film, and then a Cu wiring is formed in the groove (for example, referred to document 1).

[0006]

[Patent Document 1]

Japanese Patent Laid-Open 2000-58650

[0007]

Therefore, in conventional display devices, beaten-copper with low resistance is used for a PWB-side wiring of a printed-wiring board (PWB) in electrically connecting the PWB-side wiring to an element-side wiring with an isotropic conductive film instead of a wiring to suppress voltage drop of the element-side wiring and signal

delay (for example, referred to document 2).

[0008]

[Patent Document 2]

Japanese Patent Laid-Open 2001-236025

[0009]

[Technical Problems before the Present Invention]

It is an object of the present invention to prevent the above-mentioned influence of the voltage drop due to the wiring resistance, the trouble in writing of driving current into a pixel, and the trouble in gray scales and to provide semiconductor devices with higher definition, represented by an EL display device and a liquid crystal display device. In addition, it is also an object of the present invention to form a wiring with wiring resistance reduced in accordance with fewer processes and provide a semiconductor device that has the wiring with low resistance.

[0010]

[Means for solving the Problem]

In order to achieve the above objects, a wiring or an electrode used for display devices represented by an EL display device and a liquid crystal display device is characterized by forming by a wiring containing Cu as its main component (Hereinafter, a wire comprising Cu). In addition, "a wiring including Cu" may be formed by laminating further a wiring containing Cu as its main component (Hereinafter, a Cu wiring) over a signal line with a single-layer or a laminated-layer, a current supply line, a source electrode or a drain electrode, and a gate electrode or a scan line. In addition, the Cu wiring may be provided in a wiring with a laminate structure and a part of a layer of the electrode.

[0011]

A conductive film named functionally is the wiring or the electrode, for example, assuming a gate electrode, a source electrode, and a drain electrode of a thin film transistor (Hereinafter TFT), a signal line, a scan line, a current supply line, or the like. Since the electrode and the wiring can be obtained when a conductive film is subjected to patterning into a predetermined shape, the electrode and the wiring also collectively mean a conductive film. It is noted that the electrode is not clearly distinguished from the wiring since a portion of the signal line, the current supply line or the scan line which is assumed the wiring is an electrode.

[0012]

Such a wiring material Cu diffuses into a semiconductor film and an interlayer insulating film and has a harmful influence on electric characteristics of a TFT. In the present invention, therefore, a barrier film (a barrier layer) is provided at least between an active layer and the Cu wiring in order to prevent penetration of Cu into the active layer (a semiconductor film subjected to patterning into an island-shape) of a TFT. Such barrier film is formed of a conductive film containing nitrogen or carbon (a conductive barrier film), and one kind or plural kinds of materials selected from tantalum nitride (TaN), titanium nitride (TiN), or tungsten nitride (WN), tantalum carbide (TaC), and titanium carbide (TiC) may be used. In addition, a ternary-system amorphous barrier film containing Si may be used for the conductive barrier film.

[0013]

More preferably, a barrier film formed of an insulating film (an insulating barrier film) containing nitrogen is formed for covering the Cu wiring. For example, one kind or plural kinds of materials selected from silicon nitride (SiN), silicon

oxynitride (SiNO), and aluminum nitride (AlN, $Al_xN_y$), for example, may be used to form the insulating barrier film containing nitrogen.

[0014]

Further, the Cu wiring of the present invention is characterized by forming with sputtering. It is preferable to form the conductive barrier film, the Cu wiring, and the insulating barrier film sequentially film with sputtering.

[0015]

Fig. 11 shows an example of a specific structure of the wiring and the electrode of the present invention. In addition, an explanation will be given with Fig. 11 on a structure in which a Cu wiring formed on a conductive barrier film is covered with an insulating barrier film.

[0016]

A wiring shown in Fig. 11A has a structure in which a conductive film containing Ti, a conductive barrier film containing TiN, and Cu wiring are laminated in order from a substrate side, and an insulating barrier film containing SiN is provided for covering a laminated wiring. Hereinafter, the laminate structure is denoted as Ti/TiN/Cu/SiN from the substrate side. In this case, a width of Ti is the same as that of TiN (a length in a channel length direction) however, a width of Cu is formed shorter than widths of Ti and TiN.

[0017]

A wiring shown in Fig. 11B has a structure in which TiN is provided as a conductive barrier film and SiN is provided as an insulating barrier film and conductive films of the wiring are laminated. The laminate structure is denoted as Ti/Al/TiN/Cu/SiN from the substrate side. In this case, widths of Ti, Al and TiN are

the same, however the width of Cu is formed shorter.

[0018]

A wiring shown in Fig. 11C has a structure in which TaN is provided as a conductive barrier film and SiN is provided as an insulating barrier film the laminate structure is denoted as Ti/TaN/Cu/SiN from the substrate side. In this case, widths of Ti and TaN are the same, however the width of Cu is formed shorter.

[0019]

A wiring shown in Fig. 11D has a structure in which WN is provided as a conductive barrier film and SiNO is provided as an insulating barrier film, and the laminate structure is denoted as Ti/WN/Cu/SiNO from the substrate side. In this case, widths of Ti and WiN are the same, however the width of Cu is formed shorter.

[0020]

In short, the wiring of the present invention is formed in order that the conductive film and the conductive burrier film have the same width and the width of the Cu wiring is shorter than that of the conductive film and the conductive barrier film. The width of the conductive film and the conductive barrier film is on the order of 30 to 40 μm in a pixel portion, and it is preferable that the Cu wiring has a width on the order of 5 to 20 μm and a height on the order of 0.1 to 1 μm.

[0021]

The wiring including Cu may be used as a source electrode and a drain electrode of a TFT. In this case, a similar structure to the structures of the wirings shown in Fig. 11 may be used. Particularly, it is preferred that the wiring including Cu is used for a source electrode and a drain electrode of a TFT for supplying large current (for example, a buffer TFT of a driving circuit portion).

[0022]

The wiring including Cu may also be used as a gate electrode. In this case, the Cu wiring may be formed on the conductive barrier film. It is noted that the Cu wiring may be formed on the conductive barrier film as a scan line at the same time as the gate electrode.

[0023]

Namely, the wiring including Cu of the present invention is applicable to any of wirings and electrodes such as a signal line, a scan line, a current supply line, a source electrode, a drain electrode, and a gate electrode. Since Cu has low resistance and makes it possible to flow large current, it is possible to reduce voltage drop and a deadened signal waveform when the wiring including Cu is used. In addition, a display device that has a Cu wiring with low resistance can have an area of a wiring and an electrode reduced, and it is possible to achieve a narrowed frame. Further, it is necessary to flow large current into a wiring in a middle-sized and a large sized (5 inch or more) EL display devices and liquid crystal display devices, and therefore the present invention is useful.

[0024]

[Embodiment Modes of the Invention]

Embodiment modes of the present invention will be described below with drawings. In the description below, a transistor has three terminals of a gate electrode, a source electrode, and a drain electrode. However, it is difficult to clearly distinguish between the source electrode and the drain electrode considering a structure of the transistor. In describing a connection between elements, therefore, one of the source electrode and the drain electrode is denoted as a first electrode, and the other is denoted

as a second electrode.

[0025]

[Embodiment Mode 1]

In the present embodiment mode, the case of applying a wiring including Cu to a signal line and a current supply line will be described with reference to Figs. 1 to 4.

[0026]

Fig. 1A shows an equivalent circuit of a pixel of an EL display device. As shown in Fig. 1A, the pixel has at least a signal line 101, a current supply line 102, a scan line 103, plural TFTs 104, 105, a capacitor 106, and a light emitting element 107. The TFTs may have a multi-gate structure such as a double-gate structure or a triple-gate structure instead of a single-gate structure. It is unnecessary to provide the capacitor 106 in the case of having large gate capacities of the TFTs 104 and 105 and leakage current within the allowable range.

[0027]

Here, it is the signal line 101, the current supply line 102, and the scan line 103 that have trouble due to wiring resistance. It is necessary to consider voltage drop due to the wiring resistance in the signal line 101 and the current supply line 102 particularly as a display device has a larger size. In the present embodiment mode, a wiring including Cu is used as at least the signal line 101 and the current supply line 102.

[0028]

Fig. 1B shows a top view of Fig. 1A with a pixel electrode (a first electrode of the light emitting element) 107' formed, a Cu wiring 108 is laminated on the signal line 101 and the current supply line 102. The TFT 104 has a first electrode connected to

the signal line 101 and a second electrode connected to the capacitor 106 and a gate electrode of the TFT 105, and a portion of the scan line is a gate electrode of the TFT 104. The TFT 105 has a first electrode connected to the pixel electrode 107' and a second electrode connected to the current supply line 102. The capacitor 106 is formed in a region in which the current supply line 102 and a semiconductor film are laminated.

[0029]

Next, an explanation will be given with Fig. 2A on a structure of a sectional view along A-A' shown in Fig. 1B. Fig. 2A shows a substrate 111 with an insulating surface, and it is possible to use any of a glass substrate, a ceramic substrate, a quartz substrate, a silicon substrate, and a plastic substrate (including a plastic film) as the substrate 111. On the substrate 111, a silicon oxynitride film 112a and a silicon oxynitride film 112b are laminated as a base film. Of course, it is not necessary to limit a material of the base film to silicon oxynitride. Further, a semiconductor film (semiconductor film 113 collectively) for an active layer of the TFT 105 and for the capacitor 106 is provided on the silicon oxynitride film 103.

[0030]

The semiconductor film 113 of the TFT is covered with a gate insulating film 114, and a gate electrode of a laminate of tantalum nitride (TaW) 115 and tungsten (W) 116 is provided thereon. Although a silicon oxynitride film is used as the gate insulating film 114 in the present embodiment mode, it is useful in terms of improving an integration level to use a nitrided insulating film with a high relative dielectric constant such as an aluminum nitride film since an element space required can be reduced. Although the metal films of the gate electrode have large selection ratios

each other, such structure becomes possible when etching conditions are optimized. With respect to the etching conditions, it may be possible to refer to Japanese Patent Laid-Open 2001-313397 by the present applicant. After that, the gate electrode or resist is used as a mask to form a source region, a drain region, and a channel forming region. In addition, an LDD region and a GOLD region overlapped with the gate electrode may appropriately be formed. It is noted that the source region, the drain region, the LDD region, or the GOLD region, into which an impurity is doped, is denoted as an impurity region. Further, a heating furnace or laser is used to activate the impurity region.

[0031]

Besides, a silicon nitride film or silicon oxynitride film is provided as an insulating film 117 covering the gate electrode. In the present embodiment mode, a silicon oxynitride film is formed with plasma CVD. In addition, for planarization, a photosensitive or non-photosensitive organic material (polyimide, acrylic, polyamide, polyimideamide, resist, or benzocyclobutene), an inorganic material (such as silicon oxide, silicon nitride, or silicon oxynitride) formed with sputtering, CVD, or coating, or a laminate thereof is used to form a first insulating film 118 as an interlayer insulating film on the insulating film 117.

[0032]

On the first insulating film 118, a first passivation film 119 including a nitrided insulating film (typically, a silicon nitride film or a silicon oxynitride film) is formed. In the present embodiment mode, a silicon nitride film is used for the first passivation film 119. After that, a contact (an opening portion) in the first passivation film 119, the first insulating film 118, the insulating film 117, and the gate insulating film 114

with wet etching or dry etching.

[0033]

It is noted that the contact shown in Fig. 2A and provided in the interlayer insulating film has a tapered shape in which a diameter becomes smaller toward the bottom and an angle made by a top surface of the interlayer insulating film and a slope of the contact (a corner portion of the contact) is on the order of 95 to 135 degree. In the contact, a drain electrode or a source electrode (Hereinafter, an electrode collectively) 120 is formed to be connected a source region or a drain region. In this case, patterning of the same layer is performed to form the signal line 101 and the current supply line 102 at the same time. In the present embodiment mode, the electrode, the signal line, and the current supply line are formed of a laminate film of Ti/Al/TiN, and TiN functions as a conductive barrier film.

[0034]

Then, the Cu wiring is formed on the signal line 101 and the current supply line 102. In this case, the Cu wiring is formed by using DC sputtering with a mask. Note that it is possible to refer to Embodiment Mode 4 on detailed forming processes.

[0035]

As mentioned above, the signal line and the current supply line can be formed as the wring including Cu. That is, the Cu wiring can be formed on the signal line and the current supply line.

[0036]

Fig. 2B shows a different structure from that of Fig. 2A in which the corner portion of the contact has the tapered shape with the angle. A contact has a corner portion rounded and a diameter that becomes smaller toward the bottom. As a material

of an interlayer insulating film in this case, a photosensitive or non-photosensitive organic material (polyimide, acrylic, polyamide, polyimideamide, resist, or benzocyclobutene) may be used. Then, wet etching or dry etching may be performed after exposure to form the structure with the contact. In this case, after providing the contact in the interlayer insulating film, the first passivation film is formed.

[0037]

Further, Fig. 2C has a contact with another different tapered shape, and the contact has a corner portion rounded and a slope with two different curvature radiuses. As a material of an interlayer insulating film in this case, a photosensitive or non-photosensitive organic material (polyimide, acrylic, polyamide, polyimideamide, resist, or benzocyclobutene) may be used. Then, wet etching or dry etching may be performed after exposure to form the structure with the contact. In the case of using the photosensitive organic material, however, exposure is carried out to form the contact without etching. After providing the contact in the interlayer insulating film, the first passivation film is formed.

[0038]

The shape of the contact in the interlayer insulating film, shown in each of Figs 2A to 2C, makes it possible to prevent breaking of the wiring 102 of the capacitor 106 and the wiring 120 provided for the TFT 105.

[0039]

Then, an insulating barrier film 204 for covering the Cu wiring is preferably formed as shown in Fig. 3A. In order to form the insulating barrier film 204, a material such as silicon nitride (SiN) or silicon oxynitride (SiNO) may be used. In the present embodiment mode, a film containing silicon nitride is formed with high

frequency sputtering. Note that it is possible to refer to Embodiment Mode 4 on detailed forming processes. Since the Cu wiring is covered with the insulating barrier film 204, the risk of diffusion of Cu into the semiconductor film is further reduced.

[0040]

Then, a photomask is used to form an opening portion in the insulating barrier film 204, and the pixel electrode 107' is formed to cover the opening portion. In this case, the pixel electrode 107' is connected to the wiring 120 through the opening portion.

[0041]

It is noted that structures shown in Fig. 3B, C are different from that of Fig. 3A in a forming order of the wiring120, the insulating barrier film 204 and the pixel electrode 107' or a forming process of the opening portion in the insulating barrier film 204.

[0042]

The structure shown in Fig. 3B is different from that of Fig. 3A. The structure is that after providing the pixel electrode 107', the wiring 120, the signal line 101, and the current supply line 102 are formed, and the Cu wiring 108 is formed on the signal line 101 and the current supply line 102, and then the insulating barrier film 204 is formed and lastly, the opening portion is provided in the insulating barrier film 204.

[0043]

In the case of forming the structure of Fig. 3C, along with the case of forming the structure of Fig. 3A, the wiring 120, the signal line 101, and the current supply line 102 are formed, the Cu wiring 108 is formed on the signal line 101 and on the current supply line 102, and the insulating barrier film 204 is formed. After that, differently

from the case of Fig. 3A, an insulating film 118' as a second interlayer insulating film is formed and a second passivation film 119' is formed on the insulating film 118'. Then, an opening portion is provided in the insulating film 118' and the second passivation film 119', the pixel electrode 107' is provided in the opening portion to be connected to the wiring 120. It is noted that the insulating film 118' may be formed of the same material with the same means as the first insulating film 118 and the second passivation film 119' may be formed of the same material with the same means as the first passivation film 119.

[0044]

Further, in a structure shown in Fig. 3D, a manufacturing method of the insulating barrier film 204 is different from Figs. 3A to 3C, the structure is that after forming the Cu wiring 108, the insulating barrier film 204 is formed with a mask to cover at least the Cu wiring 108. Accordingly, it is unnecessary to provide the opening portion in the insulating barrier film 204 with the photomask.

[0045]

In this case, a conductive barrier film may be used instead of the insulating barrier film 204. This is because insulation between the pixel electrode and the conductive barrier film is ensured with a second insulating film later formed. Since the conductive barrier film has smaller capacitance compared to the insulating barrier film, the Cu wiring covered with the conductive barrier film entirely is suitable for a high-speed operation.

[0046]

It is noted that it is possible to apply the above-mentioned structure of the insulating barrier film 204 shown in Fig. 3D and the manufacturing method thereof to

the cases of Figs. 3A to 3C, and it becomes possible to use a conductive barrier film instead of the insulating barrier film 204.

[0047]

Next, an explanation will be given with reference to Fig. 4 on processes of providing a second insulating film that functions as a bank (also called a partition, or a barrier), forming an opening portion in the second insulating film on the pixel electrode, and providing a light emitting layer and the second electrode in the pixel electrode.

[0048]

In Fig. 4A, a second insulating film 205 is formed at both ends of the pixel electrode 107' of the structure shown in Fig. 3A. A photosensitive or non-photosensitive organic material (polyimide, acrylic, polyamide, polyimideamide, resist, or benzocyclobutene), an inorganic material (such as silicon oxide, silicon nitride, or silicon oxynitride) formed with CVD, sputtering or coating, or a laminate thereof is used to form the second insulating film 205. In the case of a photosensitive organic material for the second insulating film 205, one of two kinds of photosensitive organic materials classified roughly, a negative photosensitive organic material that becomes insoluble in an etchant with light or a positive photosensitive organic material that becomes soluble in an etchant with light, is appropriately used, an opening portion is formed on the pixel electrode 107', and the second insulating film 205 is formed at both ends of the pixel electrode 107'.

[0049]

After that, a light emitting layer 206 including an organic compound is formed in the opening portion, and a second electrode 207 is formed on the light emitting layer. It is preferable to perform heating under vacuum for degassing before or after forming

the light emitting layer including the organic compound. Also, it is preferable that a surface of the first electrode is planarized since the light emitting layer 206 including the organic compound is extremely thin, and for example, planarization may be performed with treatment of chemical mechanical polishing (typically, CMP) before or after patterning of the first electrode. In addition, cleaning (brush cleaning or bellclean cleaning) for cleaning foreign particles (such as dusts) may be performed in order to improve cleanness of the surface of the pixel electrode.

[0050]

It is noted that the opening portion of the second insulating film 205, shown in Fig. 4A, has a tapered shape in which a diameter become smaller toward the bottom and an angle made by a top surface of the second insulating film and a slope of the contact (a corner portion of the contact) is on the order of 95 to 135 degree.

[0051]

A structure shown in Fig. 4B is different from that in Fig. 4A in which the corner portion of the contact has the tapered shape with the degree. A contact has a corner portion rounded and a diameter that becomes smaller toward the bottom. As a material of the second insulating film, a photosensitive or non-photosensitive organic material (polyimide, acrylic, polyamide, polyimideamide, resist, or benzocyclobutene) may be used. Then, wet etching or dry etching may be employed after exposure to form the contact.

[0052]

Further, another different tapered shape of a contact is shown in Fig. 4C. The contact has a corner portion rounded and a slope with two different curvature radiuses R1 and R2. As a material of the second insulating film, a photosensitive or

non-photosensitive organic material (polyimide, acrylic, polyamide, polyimideamide, resist, or benzocyclobutene) may be used. Then, wet etching or dry etching may be employed after exposure to form the contact.

[0053]

Although Figs. 4A to C is described based on the structure shown in Fig. 3A, it is possible to combine any of the structures shown in Figs. 3B to D, and further Figs. 2A to C.

[0054]

Although the case of the display device that has the light emitting element is described in the present embodiment mode, it is needless to say that the wiring including Cu may be used as a signal line, an electrode, and other wiring in a display device that has a liquid crystal element.

[0055]

As mentioned above, in the present embodiment mode is characterized in that the wiring represented by the signal line or current supply line, the wiring including Cu (specifically, the Cu wiring provided on the wiring). Accordingly, the Cu wiring is allocable to structures and manufacturing processes of all TFTs, pixel electrodes, and wirings.

[0056]

Further, when the wiring including Cu is used in the present embodiment mode, it becomes possible to reduce voltage drop and around of a signal waveform. Additionally, it is possible to reduce an area of the wiring and the electrode and to achieve a narrowed frame in the display device that has the wiring including Cu with low resistance.

[0057]

[Embodiment Mode 2]

In the present embodiment mode, an example in which a wiring including Cu is applied to a gate electrode will be described with reference to Fig. 5.

[0058]

Fig. 5A shows an equivalent circuit of a pixel in an EL display device. As shown in Fig. 5A, the pixel has at least a signal line 601, a current supply line 602, a scan line 603, plural TFTs 604, 605, a capacitor 606, and a light emitting element 607. It is noted that the TFTs may have a multi-gate structure such as a double-gate structure or a triple-gate structure instead of a single-gate structure.

[0059]

Further, Fig. 5B shows a top view of Fig.5A in which a pixel electrode (a first electrode of the light emitting element) 607' is formed, and has the signal line 601, the current supply line 602, the scan line 603, TFTs 604, 605, the capacitor 606, and the pixel electrode 607' of the light emitting element. A Cu wiring 608 is provided on the scan line 603 and a gate electrode of the TFT 604, that is on the wiring formed of the same layer as the gate electrode.

[0060]

Fig. 5C shows a sectional view along B-B' in Fig. 5B. Similarly to Fig. 2, a substrate with an insulating surface 611, a silicon oxynitride film 612a and a silicon oxynitride film 612b as a base film, a semiconductor film 613 of the TFTs 604 and 605 are provided. Then, a gate insulating film 614 is provided to cover the semiconductor film 613, and a conductive barrier film 615 and the Cu wiring 608 are formed over the semiconductor film. Namely, the present embodiment mode is characterized in that

the wiring including Cu is used as the gate electrode. It is be possible to refer to Embodiment Mode 4 on forming processes of the wiring including Cu. The conductive barrier film 615 is formed using one selected from tantalum nitride (TaN), titanium nitride (TiN), and tungsten nitride (WN) or a laminate film of plurality thereof, and has a function as a protective film for preventing penetration of Cu due to diffusion into the semiconductor film 613. The same layer as the gate electrode is subjected to patterning to form the scan line 603 at the same time in addition to the gate electrode. That is, the scan line 603 has a laminate structure of the conductive barrier film and the Cu wiring.

[0061]

Then, a source region, a drain region, and a channel forming region are formed with gate electrode or resist as a mask. Additionally, an LDD region and a GOLD region overlapped with the gate electrode may appropriately be formed. It is noted that the source region, the drain region, the LDD region, or the GOLD region, into which an impurity is doped, is denoted as an impurity region. As an insulating film 617 covering the gate electrode, a silicon nitride film or a silicon oxynitride film is provided. The insulating film 617 functions as an insulating barrier film.

[0062]

In order to activate the impurity regions, heating furnace or laser is used. In this case, it is preferable to irradiate laser (for example, excimer laser) from a back surface (a backside of the side with the semiconductor film formed) of the substrate for the activation in order to prevent Cu from diffusing to penetrate into the semiconductor film due to heating in the activation. More preferably, the impurity regions are formed after forming the conductive barrier film 615, the heating furnace or laser is used to

activate the impurity regions, and then the Cu wiring is formed.

[0063]

In addition, for planarization, a photosensitive or non-photosensitive organic material (polyimide, acrylic, polyamide, polyimideamide, resist, or benzocyclobutene), an inorganic material (such as silicon oxide, silicon nitride, or silicon oxynitride) formed with sputtering, CVD, or coating, or a laminate thereof is used to form an interlayer insulating film 618 on the insulating film 617.

[0064]

Next, on the interlayer insulating film 618, a first passivation film 619 including a nitrided insulating film (typically, a silicon nitride film or a silicon oxynitride film) is formed. In the present embodiment mode, a silicon nitride film is used for the first passivation film 119. Then, wet etching or dry etching is used to form a contact (an opening portion) in the first passivation film 619, the interlayer insulating film 618, the insulating film 617, and the gate insulating film 614. As a shape of the contact, that is, a shape of the interlayer insulating film, any structure of Figs. 2A to 2C may be applied.

[0065]

In the contact, a drain wiring or a source wiring 120 is formed and connected to the source region or the drain region, and patterning of the same layer as the wiring forms the signal line 601 and the current supply line 602 at the same time. After that, a light emitting layer and the like are formed as shown in Fig. 3 and Fig. 4. It is noted that any structure of Figs. 3A to C may be employed for a pixel electrode to be formed and any of Figs. 4A to C may be used as a structure of an insulating film and the like for forming the light emitting layer.

[0066]

In this way, it is possible to apply the wiring including Cu to the gate electrode. It is also possible to use the wiring including Cu as the signal line and the current supply line in addition to the gate electrode.

[0067]

When the wiring including Cu is applied to the gate electrode and the scan line as set fourth above, it is possible to reduce voltage drop and a deadened waveform and further to achieve a narrowed frame of the display device.

[0068]

[Embodiment Mode 3]

In the present embodiment mode, an explanation will be given with Fig. 6 on a whole configuration of an EL (electroluminescence) display device to which the Cu wiring is applicable. Fig. 6 shows a top view of the EL display device in which an element substrate that has a TFT formed is sealed with a sealing material, Fig. 6B shows a sectional view along B-B' of Fig. 6A, and Fig. 6C shows a sectional view along A-A' of Fig. 6A.

[0069]

On a substrate 301, a pixel portion (display portion) 302 is arranged and a signal line driving circuit (source line driving circuit) 303, a scan line driving circuit (gate line driving circuit) 304a, 304b, and a protective circuit 305 are also arranged to surround the pixel portion 302. A sealant 306 is provided to surround the driving circuits. In addition, a Cu wiring 300 is provided over taken-around wirings from a signal line, a current supply line, and the signal line driving circuit to an input terminal pf FPC (flexible printed circuit). It is possible to refer to Embodiment Modes 1 and 2

on a structure of the pixel portion 303, particularly, on a structure of a wiring thereof. As a sealing material 306, glass, metal (typically, stainless), ceramics, or plastic (including a plastic film) can be used, and it is also possible to perform sealing only with an insulating film.

[0070]

Additionally, it is necessary to use a translucent material in accordance with an emission direction of light from a light emitting element. For example, light is emitted to a substrate side in the case of using a transparent electrode (ITO, for example) as the pixel electrode 107' shown in Fig. 4 while light is emitted to the opposite side to the substrate side in the case of using a transparent electrode (ITO, for example) as the second electrode 207.

[0071]

The sealant 306 may be provided to overlap with a portion of the signal line driving circuit 303, the scan line driving circuit 304a, 304b, and the protective circuit 305. The sealant 306 is used to provide the sealing material 307, and the substrate 301, the sealant 306, and the sealing material 307 are formed to form an enclosed space 308. The sealing material 307 has a desiccant 309 (such as barium oxide or calcium oxide) provided in a concave portion thereof, which has a function of adsorbing moisture and oxygen to keep clean inside the enclosed space 308 and suppress degradation of a light emitting layer. The convex portion is covered with a meshed cover material 310, and air and moisture can pass through the cover material 310 while no desiccant 309 can go through the cover material 310. It is noted that the enclosed space 308 may be filled with rare gas such as argon, and filling with inactive resin or liquid is also possible.

[0072]

In the present embodiment mode, the protective circuit 305 is provided between an input terminal portion 311 and the signal line driving circuit 303 to let static electricity such as a sudden pulse signal therebetween go outside. On this occasion, the instantaneous signal with high voltage is deadened first, and the circuit including a semiconductor film can let the deadened high voltage go outside. The protective circuit, of course, may be provided at the other position, for example, between the pixel portion 302 and the data line driving circuit 303 or between the pixel portion 302 and the scan line driving circuit 304a, 304b.

[0073]

Further, the input terminal portion 311 for transmitting a signal to the signal line driving circuit 303 and the scan line driving circuit 304a, 304b is provided on the substrate 301, and a data signal such as a video signal is transmitted to the input terminal portion 311 through FPC 312. The FPC is also connected to a taken-around wiring from a second electrode of a light emitting element and a taken-around wiring form a scan line which are not shown in the figures.

[0074]

Fig. 6B shows a section of the input terminal portion 311, and an input wiring is electrically connected to a wiring 315 provided at the FPC 312 side with resin 317 with a conductor 316 dispersed therein. The input wiring has a structure in which conductive oxide film 314 is laminated in a wiring 313 formed at the same time as the scan line (gate wiring) or the signal line (data wiring). For the conductor 316, a spherical polymer may be subjected to gold coating or silver coating.

[0075]

Fig. 7 shows an enlarged view of the input terminal portion 311 (in particular, a

portion 320 shown in Fig. 6A), specifically, shows a top view of a first wiring 701 which is a taken-around wiring for a connection with FPC formed at the same time as the signal line and the current supply line, a Cu wiring 702 provided on the first wiring, a contact 703 provided in a first insulating film, and a transparent electrode (an ITO film, for example) 704.

[0076]

Fig. 7B shows a sectional view along A-A' in Fig. 7A. First, on a wiring 706 formed at the same time as the gate wiring, the first insulating film 707 formed at the same time as an interlayer insulating film is provided. After that, the first wiring 701 as the taken-around wiring is formed in the contact (opening portion) formed in a first insulating film 707, and is connected to the scan wiring 706 through the contact. Next, on the first wiring 701, the Cu wiring 702 subjected to patterning is formed to extend in front of the contact. The transparent electrode 704 is formed to extend from a position on the first insulating film 707, and may be formed to have contact with the first wring 701. Next, a second insulating film 711 is formed over the first insulating film to cover the first wiring and the Cu wiring, and an opening portion is formed in the second insulating film 711 to cover a periphery (called also an edge or a frame) of the transparent electrode 704 and make the surface thereof exposed (the top view of the Fig. 7A). It is noted that a margin d between the first insulating film 707 and the second insulating film 711 are set to several μm, for example, 3 μm.

[0077]

Here, Fig. 7C shows an enlarged view of a protective circuit 720 and its vicinity. In the vicinity of a connecting region to the FPC (hereinafter, a connecting region), a semiconductor film including silicon formed at the same time as an active

layer of the TFT has a rectangle provided stepwise (zigzag). Then, the semiconductor film 712 is connected to the first wiring 701 and the scan line 706 through a contact to function as the protective circuit. With such protective circuit provided, the semiconductor film functions as a resistor to be able to prevent excessive current due to static electricity and the like from flowing to the driving circuit portion and the pixel portion.

[0078]

Besides, a TFT or a thin film diode may be provided instead of the semiconductor film. For example, a TFT or a thin film diode, provided to connect to a signal line (signal input line) to which a start pulse or a clock pulse input to the signal line driving circuit or the scan line driving circuit is input, may be used as a protective circuit. Of course, a plurality of semiconductor films, TFTs, or thin film diodes may be provided.

[0079]

Further, the connection between a terminal of the FPC and the taken-around wiring is different in the case of connecting the taken-around wiring to the electrode of the light emitting element from the case of connecting the taken-around wiring to the wiring of the driving circuit portion. That is, in the case of connecting the taken-around wiring to the electrode of the light emitting element, a wider width of the taken-around wiring is designed and two FPC terminals are connected with respect to the taken-around wiring since it is desired to lower resistance as much as possible. On the other hand, in the case of connecting the taken-around wiring to the wiring of the driving circuit, a narrower width of the taken-around wiring is designed, compared to the above-mentioned case, and one FPC terminal is connected with respect to the

taken-around wiring. In this way, the number of connected FPC terminals is set in consideration of the object connected to the taken-around wiring. Furthermore, the protective circuit may be provided with respect to each electrode of the light emitting elements and each wiring of the driving circuit portion.

[0080]

Then, not shown in the top view of Fig. 7A, resin 707 including a conductor 708 is formed in the opening portion of the second insulating film 711, and connected to FPC 710 through a wiring 709 provided at the FPC side.

[0081]

As set forth above, in the present embodiment mode, the Cu wiring is provided at the required position of the taken-around wiring to reduce wiring resistance, and it is possible to prevent heat from generating from the wiring. Especially, in the case of a middle-sized or a large-sized panel, it is necessary to make large current flow. Accordingly, it is useful to use the Cu wiring with low electric resistance as the present embodiment mode since there is an advantage that large current can be made to flow.

[0082]

[Embodiment Mode 4]

The Cu wiring is formed with DC sputtering, RF sputtering, or remote plasma. In the present embodiment mode, an explanation will be given with Figs. 8 to 10 on how to form the Cu wiring.

[0083]

Fig. 10 shows a multi-chamber system including a transferring chamber 35 in the center, a first deposition chamber 31 for forming a conductive barrier film, a second deposition chamber 32 for forming a Cu wiring, a third deposition chamber 33 for

forming an insulating barrier film, a takeout chamber 34 for taking a substrate out, and a loading chamber 36. The transferring chamber is connected with the respective deposition chamber respectively through transferring gates 40a to 40d. It is noted that reduced pressure is kept in the multi-chamber system at deposition.

[0084]

With the multi-chamber system as show in Fig. 10, it becomes possible to form the conductive barrier layer, the Cu wiring, and the insulating barrier film continuously without exposure to the air. When such continuous deposition is performed, it becomes possible to prevent impurities from adhering to the interface and perform favorable deposition.

[0085]

Fig. 8 shows an example of a deposition system of the second deposition chamber shown in Fig. 10. The deposition system has a deposition chamber 11 provided with a transferring port (takeout port) 22 for taking an object to be processed (a substrate) out. In the deposition chamber 11, a target of Cu 17 is provided being cooled down with a cooling medium 19 (water-cooled) through a backing plate, and circular motion or linear motion of a permanent magnet 18 in parallel directions to the target makes it possible to form a film with a favorable uniformity in a film thickness on a surface of an opposing substrate. A shutter 23 opens and closes before and after starting deposition, and prevents a film from being formed in a state with unstable plasma at the beginning of discharge.

[0086]

A substrate holder 27 and a mask holder 28 are moved to set a substrate holding means 12, a substrate 13 and a mask 14. In this case, the alignment of the

substrate and the mask may be carried out with a CCD camera 16 provided in the deposition chamber. Further, a magnetic substance (magnet) 15 is provided in the substrate holding means 12, and keeps the substrate 13 and the mask 14 fixed. In this case, in order to prevent the substrate in contact with the mask, a spacer may be provided to keep a gap (a height). Besides, a means for holding the target 17 has a means 26 for moving the target up and down to be able to control a distance between the substrate 13 and the target 17 at deposition. Of course, a means for moving up and down may be provided for the substrate holding means 12 to control a distance between the substrate 13 and the target 17 at deposition.

[0087]

In addition, a sheathed heater may be mounted as a heating means into the substrate holding means 12 and further heated rare gas (Ar gas) may be introduced from a backside of the substrate to perform heating uniformly. From a gas introducing means 21, gas such as rare gas and oxygen gas is introduced, and the pressure within the deposition chamber 11 is controlled with a conductance valve 25. A current plate 24 is provided for rectifying a current of sputtering gas. A high-frequency power source 20 is provided for the target, and high-frequency electric power is applied to perform sputtering.

[0088]

When sputtering with the configuration of Fig. 8 is employed, the Cu wiring can be formed with the target of Cu. The deposition of the Cu wiring may be carried out under the condition of heating the substrate at room temperature especially without heating. In order to further improve adhesiveness to a base, however, it is better to heat also the inside of the deposition chamber at temperatures from 100 to 300 °C,

preferably, from 150 to 200 °C. A typical frequency of the applied high-frequency electric power is 13.56 MHz.

[0089]

The first deposition chamber and the third deposition chamber also have a similar configuration to the deposition system shown in Fig. 8. In the case of forming a silicon nitride film, for example, a silicon target is used and sputtering gas of nitrogen and rare gas is used. Although a typical frequency of applied high-frequency electric power is 13.56 MHz, a higher frequency of 27 to 120 MHz may be used. As the frequency is getting increased, a chemical reaction becomes to have a priority in a mechanism of deposition, and it is expected to form a dense film with less damage to the base. The rare gas used as the sputtering gas may also be used as gas for heating the substrate, and the rare gas may be introduced from the backside of the substrate as shown in Fig.8.

[0090]

In the case of forming a TiN film for the conductive barrier film, deposition may be carried out at output power of 150 W, using sputtering gas of nitrogen and argon. Thus formed TiN film has a polycrystalline structure, and the function of preventing diffusion is enhanced due to an existence of grain boundaries. It is noted that it is possible to form a dense film to improve the property as a barrier when sputtering is performed under conditions of larger output power, an increased flow rate of argon, and a higher temperature of the substrate.

[0091]

Fig. 9 shows an example of the mask 14 used for the deposition of the Cu wiring, dotted lines indicate an arrangement of scan line driving circuits 811a, 811b, a

signal line driving circuit 812, and a pixel portion 813. It is a mask 800 in the case of forming the Cu wiring over a taken-around wiring, a signal line, and source and drain electrodes of a buffer TFT provided in the signal line driving circuit 811 that Fig. 9 shows. Accordingly, the mask 800 has a slit 801 for the taken-around wiring, a slit 802 for the signal line, and a slit 803 for the source electrode and the drain electrode formed. It is noted that the slits has a width of 5 μm or more, and the width may appropriately be set for a Cu wiring with a narrow width of 5 to 20 μm provided for the signal line in the pixel portion and a Cu wiring with a broad width of 150 to 1000 μm provided for the taken-around wiring. Additionally, it is preferable that a section of the slit has a taper shape toward the substrate in order to improve accuracy of deposition.

[0092]

It is noted that the mask has, for reinforcing, an auxiliary wiring 804 provided in a direction perpendicular to the slit. In order not to become a barrier at deposition, the auxiliary wiring 804 may have a width and a length appropriately set and may be arranged appropriately. At deposition of the Cu wiring, the auxiliary wiring is fixed not to face the substrate, that is, at the opposite surface of the mask to the surface facing the substrate. With such auxiliary wiring, it is possible to prevent a wiring to be formed from varying in width and meandering. The mask described above is formed of nickel, platinum, copper, stainless, or quartz glass. In particular, a mask formed of a metal material is called a metal mask. Besides, it is preferred that the mask is formed to have a thickness on the order of 5 to 25 μm although the thickness depends on a width of a wiring to be formed.

[0093]

With the deposition method as set forth above, the Cu wiring of the present

invention can be formed. Then, it is possible to reduce wiring resistance and manufacture a display device with less heating.

[0094]

[Embodiment Mode 5]

Electronic devices, each using a display device according to the present invention, include a video camera, a digital camera, a goggles-type display (head mount display), a navigation system, a sound reproduction device (such as an in-car audio system and an audio set), a lap-top computer, a game machine, a portable information terminal (such as a mobile computer, a cellular phone, a portable game machine, and an electronic book), an image reproduction device including a recording medium (more specifically, an device which can reproduce a recording medium such as a Digital Versatile Disc (DVD) and display the reproduced image), and the like. In particular, it is preferable that the Cu wiring according to the present invention is used for an electronic device with a large-sized screen such as a large-sized television. Fig. 12 shows a specific example of such electronic devices.

[0095]

Fig. 12A illustrates a large-sized display device which includes a casing 2001, a support table 2002, a display portion 2003, a speaker portion 2004, a video input terminal 2005 and the like. The wiring including Cu of the present invention can be used as a wiring and an electrode provided in the display portion 2003 to complete the large-sized display device shown in Fig. 12A according to the present invention. It becomes possible to enhance a reduction of voltage drop and a deadened signal in the large-sized display device with a long wiring length when the wiring including Cu is provided to achieve lower resistance. The display device includes all display devices

for displaying information, such as a personal computer, a receiver of TV broadcasting and an advertising display.

[0096]

Fig. 12B illustrates a lap-top computer which includes a main body 2201, a casing 2202, a display portion 2203, a keyboard 2204, an external connection port 2205, a pointing mouse 2206, and the like. The wiring including Cu of the present invention can be used as a wiring and an electrode provided in the display portion 2203 to complete the lap-top computer in Fig. 12B according to the present invention.

[0097]

Fig. 12C illustrates a portable image reproduction device including a recording medium (specifically, a DVD reproduction device), which includes a main body 2401, a casing 2402, a display portion A 2403, another display portion B 2404, a recording medium (DVD or the like) reading portion 2405, an operation key 2406, a speaker portion 2407 and the like. The display portion A 2403 is used mainly for displaying image information, while the display portion B 2404 is used mainly for displaying character information. The wiring including Cu of the present invention can be used as a wiring and an electrode provided in the display portions A and B 2043 and 2404. The image reproduction device including the recording medium further includes a home game machine or the like.

[0098]

It is noted that light including output image information is enlarged and projected with a lens or the like, and it can be used for a front-type or rear-type projector

[0099]

Further, it is necessary to supply an accurate signal to a light emitting portion

of a light emitting device since the light emitting portion consumes electric power. Accordingly, the wiring including Cu of the present invention may be used for the mobile information terminal.

[0100]

As set forth above, the present invention can be applied quite widely to electric apparatus in various fields. Besides, the electric devices in the present embodiment mode can use any of structures shown in Embodiment Mode 1 to 4.

[0101]

[Effect of the Invention]

As set fourth above, it is possible according to the present invention to use the wiring including Cu as any of wirings and electrodes such as a signal line, a scan line, a current supply line, a source electrode, a drain electrode, or a gate electrode. With Cu that has low resistance and makes it possible to flow large current, it is possible to reduce voltage drop and a deadened signal waveform. In particular, it is effective to use the wiring including Cu of the present invention for a middle-sized or a large-sized panel. In addition, a display device that has the wiring including Cu with low resistance can have an area of a wiring and an electrode reduced, and it is also possible to achieve a narrowed frame.

[0102]

Further, in the present invention, sputtering with a mask is employed to be able to manufacture the Cu wiring with high precision. Accordingly, it is unnecessary to employ complicated processes such as damascene, and it is possible to provide a display device with a low cost and a high yield.

[Brief Description of the Drawings]

[Fig. 1] A diagram that shows a display device according to the present invention.

[Fig. 2] A diagram that shows a sectional view of a pixel of a display device according to the present invention.

[Fig. 3] A diagram that shows a sectional view of a pixel of a display device according to the present invention.

[Fig. 4] A diagram that shows a sectional view of a pixel of a display device according to the present invention.

[Fig. 5] A diagram that shows a display device according to the present invention and a sectional view thereof.

[Fig. 6] A diagram that shows a display device according to the present invention and a sectional view thereof.

[Fig. 7] A diagram that shows a display device according to the present invention.

[Fig. 8] A diagram that shows a display device according to the present invention.

[Fig. 9] A diagram that shows a mask for forming a wiring according to the present invention.

[Fig. 10] A diagram that shows a deposition system for forming a wiring according to the present invention.

[Fig. 11] A diagram that shows a wiring according to the present invention.

[Fig. 12] A diagram that shows an electronic device that uses a display device according to the present invention.

Fig. 9 is Fig. 10 is a diagram that shows a deposition system for forming a wiring according to the present invention;